

ABSTRACT OF THE DISCLOSURE

An SDRAM and method for operating it provide for increased data access speed. The SDRAM includes a central memory region with memory blocks arranged in sets on respective opposite sides. A plurality of primary
5 sense amplifier sets are provided, each set being associated with a respective pair of the memory blocks and located adjacent thereto. A row cache is provided in the central memory region, and row decoders decode a row address in response to a "bank activate" command and move data from a decoded row address into a primary sense amplifier set associated with a
10 memory block containing the decoded row address and into the row cache, prior to application of a "read" command to the SDRAM. Column decoders decode a column address in response to a "read" command and for reading data from the cache in accordance with the decoded column address.